

# Firmware Build FW1038 FF1243 (03.06.2012)

**DspFirmware: Build 1038** 

Release Date: 2013-05-28 13:59:00 +0200 (Mo, 03 June 2013)

**SVN Revision:** Revision: 15127 **RLID:** 4&5&6 & 16

Remarks: supporting RevB&RevC and TSP350&700 Drives, using new PWM interface

### Changes since last Build:

- NEW: TSP350/700 adjust brake voltage depending on BridgeVoltage upperLimit param
- NEW: implemented FW download for TSx5x RevD drives
- CHG: allow setOperational if drive is already in operational state
- CHG: prevent from noisy limit cycles (standstill) if using digital encoder
- CHG: get the user a chance to reset NoValidTamaCodeAvailable fault within disabling persistent tama start options
- CHG: allow velocity = 0 for discrete and continuous moves
- CHG: allow changes of path planner parameters if not moving or if moving path will be reprogrammed immediately
- CHG: reject unimplemented Torque move commands
- CHG: speedup FW download within less protection accesses
- CHG: prepared speedup FW download (program used bytes only)
- CHG: removed support for unused SST flash chip
- FIX: correct implementation of combined drive command (ResetFault and SwitchOn)
- FIX: correct offset check in register read/write (upper level check was wrong)
- FIX: do not watch STO bits if hardware is TS150..TS351 Rev B

## SPECIAL VERSION (not released)

- 1038\_1 implementation for special summation inputs via TamVars for iD with TamVar2, iQwith TamVar3 and position X with TamVar4. Do not use TamVars(2..4) in Tama prog if FW 1038\_1 is installed!
- 1038\_2 implementation for compensation of nonlinear PWM output using TamVar0(y0) and TamVar1(u0). Do not use TamVar0&1 in Tama prog if FW 1037\_8 is installed!

FpgaFirmware: Build 1243

Release Date: 2013-05-28 13:59:00 +0200 (Mo, 03 June 2013)

# Changes since last Release:

- TLC100 reset behaviour bugfix. Adding ready led to the TLC100 device
- TAD4 support
- Refactoring of the Tria-Link fifos and router (reset behaviour)
- Trialink router: broadcast to broadcast skip
- Trialink Status/Control bugfix (Unresolved timeout)
- new hardware type TLO300 (PciE trialink master with USB observer)
- refactoring of the table feeder (thread safe control and status signals)
- refactoring of the encoder analog signal logger with more memory and trigger
- monitor communication with 32 bit crc calculation and automatic detection of the communication mode
- TL300 Rev. 0 release, TL300 Rev. Z no longer supported
- new hardware type TLO100 (Pci Tria-Link master with USB observer)
- refactoring of encoder autocalib (removal of old style external encoder calibration)
- new encoder latching features in encoder device:
  - analog and digital encoder latching with selectable index marker source
  - analog encoder fast phase signal logging
- refactoring of the encoder position filter
- refactoring of the current filter
- refactoring of the digital in/out routing
- position and current filter device with multiple filter selection
- pwm soft turn off time reduced from 10us to 1us
- time stamp starts at 0xFE001F00. This leads to the first wrap after 335s, the next wrap will be 12h later.
- the pci interface time stamp update rate changed from 100us to 10us.



# Firmware Build FW1037 FF1159 (22.10.2012)

**DspFirmware: Build 1037** 

Release Date: 2012-10-05 15:50:17 +0200 (Fr, 05 Okt 2012)

**SVN Revision: Revision:** 14015 **RLID:** 4&5&6 & 16

Remarks: supporting RevB&RevC and TSP350&700 Drives, using new PWM interface

### Changes since last Build:

- NEW: implemented modulo handling on actual position in disabled state
- CHG: rework on multi axes move commands (removed serialization)
- CHG: changed startup setting default addresses (1,xff,xff)xff)
- CHG: implemented BridgeVoltageWarning behavior in ReadyToSwitchOn state. Changed drive state machine, added startup state, event ResetFault leads to NotReadyToSwitchOn state now (see SWSCN001 DriveWarningConcept EP002.pdf for more informations)
- CHG: update watchPllNotLockedFault flag if startup setting have changed
- CHG: update and change timestamp source if timestamp startup setting have changed
- CHG: changed implementation of flash access due to thread safety problems
- FIX: improved handover of events from async to sync task. (prevents from losing events)

## SPECIAL VERSION (not released)

- 1037\_1 implementation for special summation inputs via TamVars for iD with TamVar2, iQwith TamVar3 and position X with TamVar4. Do not use TamVars(2..4) in Tama prog if FW 1037\_1 is installed!
- 1037\_2 implementation for compensation of nonlinear PWM output using TamVar0(y0) and TamVar1(u0). Do not use TamVar0&1 in Tama prog if FW 1037\_2 is installed!

FpgaFirmware: Build 1159

Release Date: 2012-07-02 12:11:02 +0200 (Mo, 02 Jul 2012)

- 1) TSP700 center control error level increased from 36V to 72V
- 2) Encoder analog filter configurable by encoder local bus register 0x43. Default is 0xC, can be set to 0x9 or 0xA to increase the encoder counting frequency up to 600kHz.



# Firmware Build FW1036 FF1159 (not released)

**DspFirmware: Build 1036** 

Release Date: Date: 2012-08-30 07:42:58 +0200 (Do, 30 Aug 2012)

**SVN Revision: Revision:** 13919 **RLID:** 4&5&6 & 16

Remarks: supporting RevB&RevC and TSP350&700 Drives, using new PWM interface

## Changes since last Build:

- version number DSP FWID increased to 1036

- CHG: improved check for overcurrent in mbc TwoBrushDCMotors (check i1, i2 and i1+i2)
- NEW: implemented special feature for compensation of nonlinear PWM output

# SPECIAL VERSION (not released)

- 1036\_1 implementation for special summation inputs via TamVars for iD with TamVar2, iQwith TamVar3 and position X with TamVar4. Do not use TamVars(2..4) in Tama prog if FW 1036\_1 is installed!
- 1036\_2 implementation for compensation of nonlinear PWM output using TamVar0(y0) and TamVar1(u0). Do not use TamVar0&1 in Tama prog if FW 1035\_2 is installed!

FpgaFirmware: Build 1159

Release Date: 2012-07-02 12:11:02 +0200 (Mo, 02 Jul 2012)

- 1) TSP700 center control error level increased from 36V to 72V
- 2) Encoder analog filter configurable by encoder local bus register 0x43. Default is 0xC, can be set to 0x9 or 0xA to increase the encoder counting frequency up to 600kHz.



## Firmware Build FW1035 FF1159 (02.07.2012)

**DspFirmware: Build 1035** 

Release Date: 2012-07-02 12:11:02 +0200 (Mo, 02 Jul 2012)

SVN Revision: Revision: 13578 RLID: 4&5&6 & 16

Remarks: supporting RevB&RevC and TSP350&700 Drives, using new PWM interface

### Changes since last Build:

- version number DSP FWID increased to 1035
- NEW: added math function sin, cos, log and log10 without hw loops to the float40Lib
- CHG: added dependency of VirtualMachineLib from Float40Lib (new NoHwLoop math functions)
- CHG: made Flaot40Lib and VirtualMachineLib independent on registerLib
- CHG: use math functions sin, cos, log and log10 without HwLoops in VM code
- CHG: use math functions without HwLoops in filter calculation
- CHG: made errno support in VM working (sqrt of neg number)
- CHG: do not automatically restart VM after VM fault if VM is not in NoStack state
- CHG: prevent from zero division if encoderPitch is 0
- CHG: removed unneeded rounding in path planner modulo handling (rounded twice)
- CHG: moved internal scheduling counter inc to the end of the highPrio part (compatible)
- CHG: perform highSpeed data sampling after call of CC to get samples from the same time slot
- CHG: adjusted the i2t current and peak current limits for all drive types
- CHG: removed Field\_Weakening debug compiler option (use

## TWO STAGE CONTROL AND FIELD WEAKENING if needed)

- CHG: implemented SafeTorqueOff Active and Inconsistent state
- CHG: changed phase advance times to match timing changes in FPGA
- INT: added debug option for highPrio timing checks
- INT: removed all asserts(), checked and reordered project options
- INT: added assert() in PPP. This solves mystery computing problem if update modulo max
- INT: added debug feature for phase advance
- FIX: spurious high prio interrupts calling the high prio task occured in special timing constellations. (t highPrio + t lowPrio ~ 10us) fixed in OS
- FIX: prevent from uninitialized currentLimit in 2DC configuration (wrong CurrentLimitXXX Error)

#### SPECIAL VERSION (not released)

- 1035\_1 implementation for special summation inputs via TamVars for iD with TamVar2, iQwith TamVar3 and position X with TamVar4. Do not use TamVars(2..4) in Tama prog if FW 1035\_1 is installed!

FpgaFirmware: Build 1159

Release Date: 2012-07-02 12:11:02 +0200 (Mo, 02 Jul 2012)

- 1) TSP700 center control error level incresed from 36V to 72V
- 2) Encoder analog filter configurable by encoder local bus register 0x43. Default is 0xC, can be set to 0x9 or 0xA to increase the encoder counting frequency up to 600kHz.