Firmware Build_FW1051_FF1544 (28.02.2018)

DspFirmware: **Build 1051**
Release Date: **$Date: 2018-02-28 14:03:19 +0100 (Mi, 28 Feb 2018) $**
SVN Revision: **$Revision: 26973 $**
RLID: **4&5&6 & 16**
Remarks: **TSx5x RevB,RevC&RevD and TSP350&700 Rev0,Rev1 Drives,**

New features:
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Bug Fixes:
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Changes:
- use new generated, separated registerLayout4_5_6 files instead of merged file

FpgaFirmware: **Build 1544**
Release Date: **2018-04-09**

New features:
- Sigma-Delta 2nd order replaced by 1st order
- Trialink Master Oscillator

Refactoring:
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Bug Fixes:
- PLL Locked threshold level changed from -64...63 to -512...511 due to problems with thermal caused frequency jumps. these jumps leaded to a trialink unlocked state throwing an error. The new threshold value is a going back to the threshold of FW1302.