

Firmware Build_FW1054_FF1563 (08.11.2018)**DspFirmware: Build 1054****Release Date: \$Date: 2018-11-06 10:05:14 +0100 (Di, 06 Nov 2018) \$****SVN Revision: Revision: 28697 \$****RLID: 4&5&6 & 16****Remarks: supporting TSx5x RevB,RevC&RevD and TSP350&700 Rev0,Rev1 Drives,****New features:**

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Bug Fixes:

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Changes:

- Allow to reset an axis error in axis state Standstill (allows to reset stream interpolator errors)

FpgaFirmware: Build 1563**Release Date: 2018-11-08****New features:**

- PLL plot signals using encoder phase A and B
 - encoder device, Address 0x40 [19:16]
 - 0x0 => uncalibrated encoder phase A
 - 0x1 => calibrated encoder phase B
 - 0x2 => encoder phase A offset C1
 - 0x3 => encoder phase A amplitude A11
 - 0x4 => encoder phase A cross-amplitude A12
 - 0x8 => pll phase error
 - 0x9 => pll phase count of ring 1
 - 0xA => ethernet intermediate gap length of ring 1
 - 0xB => ethernet frame length of ring 1

- encoder device, Address 0x40 [23:20]
- 0x0 => uncalibrated encoder phase B
- 0x1 => calibrated encoder phase A
- 0x2 => encoder phase B offset C2
- 0x3 => encoder phase B amplitude A22
- 0x4 => encoder phase B cross-amplitude A21
- 0x8 => pll frequency
- 0x9 => pll phase count of ring 2
- 0xA => ethernet intermediate gap length of ring 2
- 0xB => ethernet frame length of ring 2

Refactoring:

- ethernet frame tolerance set to +/-160ns
- ethernet gap tolerance set to +/-320ns
- timestamp crc error counted as a packet crc error
- frame error, gap error and crc error of packets counted once every 100us
- physical link device, see local bus description

Bug Fixes:

- pll not locked error when one timestamp with crc error occurs. this throws an error to the drive stopping the motion. Changed to pll not locked error when multiple timestamp with crc error occurs. "multiple" is programmable from 1 to 128 with default of 32.
- crc calculation of ethernet rx and tx divided into two calculation steps to avoid wrong crc calculation when fpga device gets hot.



Triamec Motion AG Firmware ReleaseNotes